IN THE UNITED STATES PATENT AND TRADMARK OFFICE

In Re Application of:	Date: September 29, 2010
Francois Le Maut, et.al	Customer No. 25299
Serial No. 10/22,900	Group Art Unit: 2465
Filed: November 26, 2003	Examiner: Houshmand, Hooman

FOR: SYSTEM AND METHOD FOR RE-SEQUENCING DATA PACKETS ON A PER-FLOW BASES

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
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RESPONSE TO OFFICE COMMUNICATION OF AUGUST 2, 2010

Dear Sir:

This paper is responsive to the Office Communication of August 2, 2010. The Office Communication is issued pursuant to 37 CFR 1. 105 requiring applicant and the assignee of this application to provide concise explanation of the subject matter and support in the specification and drawings, if any, for each of the Claims 1-30.
The Claims in this paper are clean copies of the ones submitted in the Amendment after Final, filed 02/16/2010, and has been entered. The response to this Office Communication begins on page 2 of this paper.

CLAIM 1

The subject matter of this Claim provides a system for resequencing per flow data packets received by at least one destination egress adapter. The Claim recites:

a plurality of output registers(500, Fig. 5,page 5, lines 25-30) with each register dynamically assigned (page 5, lines 28-29) to store received data packets(460, Fig.4,page 15, line 6)from one of a plurality of flows;

a packet buffer (465, Fig.4, page 14, line 8);

means (271,Fig. 2, page 12, line 20-24 as amended by Amendment of 9/01/2009,Fig. 6,showing flow chart of incoming packet process and describe at page 20, line 5 through page22, line 27) for allocating a temporary storage location in the packet buffer for each received data packet (Comments: The egress controller 271 could be a programmable computer, ASIC, PLA, or other circuit arrangements program and/or design according to teachings of the flow chart and related description to load packets from flows into the packet buffer);

means 19,line 5) using predefined parameters, for pointing to an output register (540) previously assigned to receive data packets from a corresponding flow (Comments: The CRI CAM 510 includes a plurality of entries. Each entry has a search area 515 and Cross Reference Index (CRI) bit 520 which identify an output register assigned to handle a flow); and

means (Egress controller 271 executing part of the flow chart 640 and 642 Fig.6, page 20, line 25 through page 21, line 10) coupled to the allocating means and to the pointing means for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register.

Claim 2

The system of claim 1 wherein the means for pointing to an output register comprise a first Content Addressable Memory (510, Fig.5, page 17, lines 15-26) wherein each entry (512, Fig.5) includes a search field (515, Fig. 5) having a source identifier, a routing index and a priority level, and an associated identifier field including a Cross Reference Index (520, Fig. 5)to point to a previously assigned output register among a plurality of output registers (500, Fig. 5).

Claim 3

The system of claim 2 wherein the identifier field further contains an activity identifier (521, Fig 5) to indicate when a previously assigned output register is no longer active, and a packet sequence number (522, Fig.5) equal to the last packet sequence number received for the corresponding flow.

Claim 4

The system of claim 2 wherein the means for pointing further comprise means (Fig.5, Free Register List (FRL)550,PAGE 17, line 27 through page 18, line 2) for

providing a new output register to each new flow of data packets.

Claim 5

The system of claim 2 wherein the first Content Addressable Memory further comprises means (Time stamp (TS) 523, Activity A bit 521,Fig. 8 Flow chart, page 25, lines 21-30) for preventing over filling of said first Content Addressable Memory (Comment: A background task executed on the controller interrogates A and TS. Depending on the state of A and TS associated entries can be deleted from the CRI CAM).

Claim 6

The system of claim 2 further comprising a second Content Addressable Memory (400) wherein each entry including a source identifier (415) a routing index (420)a priority level (425) and the packet sequence number (430) of each stored data packet, and an associated identifier field (435) to give a packet buffer identifier (ID) that identifies the storage location allocated to each received data packet (Comment: All references are in Fig. 4, and describe at page 14, line 5 through page 16, line 6).

Claim 7

The system of claim 1 wherein each of the output registers (500, Fig. 5 further comprises:

a packet sequence number (501) and a packet buffer identifier (502) for an in-process data packet; and

a valid-bit latch (505) to set an active/not active status that indicates if the in-process data packet is already output (Comment: All references are to Fig. 5, describe at page 16, line 7 through page 20, line 4).

Claim 8

The system of claim 7 wherein the output register further comprises a counter (503)to maintain a value for, each flow, the number of data packets stored in the packet buffer waiting to be transmitted.

Claim 9

The system of claim 7 further comprising scheduling means (packet scheduler 280, Fig. 2, page 18, line 30) coupled to the determination means for selecting one of the in-process data packets to be output.

Claim 10

A system for resequencing per flow data packets (460, Fig.4) received by at least one destination egress adapter (260, Fig. 2) comprising:

a plurality of output registers (500, Fig. 5) with each register dynamically (page 16, lines 28-30) assigned to store received data packets (460, Fig. 4) from one of a plurality of flows, wherein each of the output registers further comprises:

a packet sequence number (501) and a packet buffer identifier (502) for an in-process data packet; and

a valid-bit latch (505) to set an active/not active status that indicates if the in-process data packet is already output;

means (egress controller 271, page 12, lines 20-24 as amended by Amendment dated September 1, 2009 and flow chart (Fig. 6, page 6, line 5 page 22, line 28) for allocating a temporary storage location in a packet buffer (465) to each received data packet (Comments: The egress controller 271 executing process according to the flow chart (Fig. 6) allocates storage location in the buffer);

means (Fig. 5, CRI CAM 510, page 17,line 15 through page 19, line 5), using predefined parameters, for pointing to an output register (540) previously assigned to receive data packets from a corresponding flow; and

means (egress controller 271, executing part of the flow chart in Fig. 6) coupled to the allocating means and to the pointing means (Fig. 5, CRI CAM 540) for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc, PSNh) used by the pointed output register and scheduling means (280, Fig. 2) coupled to the determination means (egress controller 271, executing a process based upon part of the flow chart in Fig. 6) for selecting one of the in-process data packets (page 22, lines 28-31) to be output, wherein the scheduling means (280)is coupled to each of the valid-bit latches (Fig. 5, 505)to select (page 22, line28 through page 23, line 10)one valid-bit latch having an active status.

Claim 11

The system of claims 1 or 2 wherein the means for allocating comprise a free buffer list (Fig. 4, 470) to allocate a free temporary storage location (ID) to each received data packet (460).

Claim 12

The system of claims 1 or 2 wherein the data packets comprise unicast and multicast data packets (page 7, lines 1-3).

Claim 13

The system of claim 1 further including at least one ingress adapter (Fig. 2, 200, page 9, line 5) comprising counting means (210, Fig. 2, 360, 385 and 395 Fig. 3,page 12,line 25 through page 14, line 4) for sequentially numbering data packets of a same flow (Comments: Packet Sequence Numbers are stored in look up table (LUT) 360,increment by 1 at INCR 385 (mislabeled 395) and returned 395 to the same address in LUT 360. The device in charge of managing the node controls the action).

Claim14

The system of claim 13 wherein the ingress adapter further comprises means (load balancer circuit 205, Fig.2, page 9, line 3 through page 10, lines 1-5) for load balancing the data packets over a plurality of independent switching planes.

Claim 15

A system for resequencing per flow data packets received by at least one destination egress adapter comprising:

a plurality of output registers (500, Fig.5) with each register dynamically assigned to store received data packets from one of a plurality of flows;

means (egress controller 271 executing a part of flow chart Fig. 6) for allocating a temporary storage location in a packet buffer to each received data packet~~s~~;

means (CRI CAM 510), using predefined parameters, for pointing to an output register previously assigned to receive data packets from a corresponding flow; and

means (egress controller 271 executing another part of Flow chart in Fig. 6) coupled to the allocating means and to the pointing means (CRI CAM 510) for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register and at least one ingress adapter comprising counting means (210, 360,385 node control device as explained above) for sequentially numbering data packets of a same flow for load balancing the data packets over a plurality of independent switching planes; and

means (scheduler 220, Fig. 2) for scheduling the switching of the data packets over the plurality of independent switching planes (250), Fig.2 page 9, line 6).

Claim 16

A method for resequencing per flow data packets received by at least one destination egress adapter (260) comprising:

allocating a temporary storage location in a packet buffer (465, Fig.4) to each received data packet;

providing a plurality of output registers (500, Fig. 5) with each register dynamically assigned to store received data packets from one of a plurality of flows;

extracting predefined parameters from said each received data packets;

using the predefined parameters to search a memory (510, Fig. 5) and identifying a cross reference index;

using the Cross Reference Index associated with each received data packet to point (625, Fig 6) to a respective output register previously assigned to the corresponding flow of each received data packet; and

comparing (640, Fig. 6, page 21, line 3) a packet sequence number of each received data packet to a packet sequence number stored in the respective pointed output register to determine if said each received data packet is the next in sequence.

Claim 17

The method of claim 16 further comprising:

assigning (660, Fig. 6, page 21, lines 23 -26 and page 22, lines 5-13) a new output register and a new Cross Reference Index if no associated Cross Reference Index is found for a received data packet; and

storing (690, Fig. 6, page 21, lines 3-10) in the new output register the packet sequence number (PSN) of said received data packet.

Claim 18

The method of claim 16 further comprising checking if the assigned output register is active (This is done by checking status of A bit 621 and 622 page 20, lines 14-24).

Claim 19

The method of claim 18 further comprising:

assigning (Fig.6, 650,page 21, lines 19-29) a new output register if the assigned output register is found inactive;

comparing (Fig. 6, 655, page 21, line30) the packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register; and

storing (Fig. 6, 690,page 21, lines 26-29) in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise

storing (Fig. 6, 670, page 21, line 32) in the new output register the last packet sequence number (PSNh) used by the inactive assigned output register.

Claim 20

The method of claim 16 or17 further comprising releasing unused Cross Reference Index after a predetermined time interval.

Claim 21

A method for resequencing per flow the data packets received by at least one destination egress adapter (Fig. 2, 260) comprising:

allocating (Fig. 6, 605, page 20, line 11) a temporary storage location in a packet buffer (Fig. 2, 260) to each received data packet;

extracting predefined parameters (Fig. 6, 610, page 21, line 13) from said each received data packets;

using the predefined parameters to search (Fig. 6, 615)a memory (CRI CAM 510 Fig. 5) and identifying a cross reference index (CRI Fig 5);

using the Cross Reference Index associated with each received data packet to point (Fig. 6, 625,page 20, lines 17-20) to a respective output register previously assigned to the corresponding flow of each received data packet; and

comparing (Fig. 6, 640, page 20, lines 25-30) a packet sequence number of each received data packet to a packet sequence number stored in the respective pointed output register to determine if said each received data packet is the next in sequence;

checking if the assigned output register is active (This is done by checking status of A bit Fig. 6, page 20, lines 14-19);

assigning (Fig. 6, 650, page 22, lines 10-14) a new output register if the assigned output register is found inactive;

comparing (Fig. 6, 640, page 21, line 3)e packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register;

storing (Fig. 6, 690, page 21, lines 26-29) in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise

storing (Fig. 6, 670, page 21, lines 30-32) in the new output register the last packet sequence number (PSNh) used by the inactive assigned output register and a packet buffer identifier that identifies the storage location (ID) allocated to each received data packet.

Claim 22

The method of claims 16 or 17 further comprising writing in a Content Addressable Memory, a source identifier, a priority level and the packet sequence number of each received data packet that is not the next in sequence (Fig. 6, 685, page 21, lines 11-29), the write address being identified by the storage location allocated to said each received data packet.

Claim 23

The system of claims 1 wherein the predefined parameters include Priority Level (PTY), Routing Index (RI) and Source Identifier (Search Field 515, Fig. 5, page 17, lines 20-26).

Claim 24

A method comprising:

providing a plurality of registers (Fig. 5, 500,page 17, lines 15-20) with each register associated with a flow;

providing a cross reference table (Fig. 5, 510, page 17, lines 15-20) with each entry associated with a register within said plurality of registers;

receiving a packet(Fig. 6, 600, page 20, line 7);

searching the cross reference table with parameters selected from the packet(Fig. 6, 610 and 615, page 20, 11-14);

if a match is found, correlating at least one parameter identified in a register associated with said matching entry with parameter in the packet to determine sequence of said packet relative to a packet identified in said associated register (Fig. 6, 640, page 21' line 3-10).

Claim 25

The method of claim 24 further including if a match is not found making a new entry for said packet in said cross reference table and associating a register from said plurality of registers with said packet and flow to which the packet belongs (page 22, lines 5-13).

Claim 26

The method of claim 24 further including if the packet is in sequence with packet identified in said associated register setting a valid bit to post request for service to egress scheduler (Fig. 6, 690, lines page 21, lines 3-10).

Claim 27

The method of claim 24 further including if the packet is out of sequence relative to the packet identified within said associated register reset a valid bit indicating no request is posted to egress scheduler (Fig. 6, 670, page 21, line30-page22, line 4).

Claim 28

A computer readable medium embodied with a computer readable code (page 12, lines 20-24 as amended by Amendment of September 1, 2009) said computer readable code including a first instruction module with instructions to examine a packet and extract a set of predefined parameters therefrom (Fig.6, 610, page 20, line 13);

a second instruction module (Fig. 6, 615) with instructions that use the extracted predefined parameters to search an index table (page 20, lines 13-14, CRI CAM 510, Fig. 5) having a plurality of entries with each entry associated with a different register; and

a third instruction module (Fig. 6, 640, page 20, line 25-page 21 line 2) having instructions that correlate parameters in said packet with parameters stored in an associated register to determine sequence of said packet to packet identified in said register, if a match is found between the extracted predefined parameter and an entry in said index table (Fig. 6, 615 and 616,page 20, lines 13-17).

Claim 29

The computer readable medium of claim 28 further including a fourth instruction module (Fig. 6, 660, page 22, lines 5-14) including instructions for adding an entry for said packet to the index table if a match is not found.

Claim 30

An apparatus comprising:

a plurality of switching planes (Fig. 2, 250, page 9, lines 6-7);

a buffer (Fig. 4, egress buffer 465, page 14, line 8) for storing packets transported through said switching planes;

a system (Fig. 2, 270) for ensuring packets are in predefined sequence said system including a register stack (Fig. 5, 500, page 16, lines 25-28) wherein each register is associated with a different flow of a multi flow system;

a cross reference index table (Fig. 5, CRI CAM 510) having a plurality of entries with each entry associated with a different register in said register stack; and

a controller (egress controller 271,page 12, lines 20-24, as amended by Amendment of September 1, 2009) that selects parameters (Fig. 6, 610)from a received packet (Fig. 6, 600) to search the index table (Fig. 6, 615) and determine sequence of said packet relative to a packet identified in a register associated with a match entry.

CONCLUSION

It is believed the present amendment answers all issues raised in the subject Office communication. Reconsideration is hereby requested and an early allowance of Claims 1-30 is solicited.

Respectfully Submitted,

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